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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
FOWLKES, ANDRE R	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,774	ROBISON, ARCH D.	
	Examiner	Art Unit	
	Andre R. Fowlkes	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed 2/6/06.

2. Claims 1-28 are pending. Claims 1, 8, 9, 15, 22 have been amended.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, there is no support given from the original disclosure for the limitation "identifying, prior to register allocation, a plurality of unifiable variables" in claims 1, 8, 15, and 22. There is no listing of the page and line numbers, from the specification, in support of each change in the amended claims, in the remarks. Additionally, the examiner could not locate this limitation within the specification.

To overcome this objection, applicant may attempt to demonstrate that the original disclosure establishes that he or she was in possession of the amended subject

matter or **provide the page and line numbers, from the specification, in support of each change in the amended claims.**

Accordingly, claims 2-7, 9-14, 16-21 and 23-28 are rejected as being dependent on a rejected base claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper, et al., (Cooper), "Enhanced Code Compression for Embedded RISC Processors", SIGPLAN '99, in view of Damron et al., (Damron), U.S. Patent No. 6,918,111.

As per claim 1, Cooper discloses a method comprising:

- identifying, prior to register allocation, a plurality of fork subgraph structures within a graph structure constructed for a plurality of executable instructions (p. 143 col. R:23-24, "we first use the interference graph to (identify a plurality of fork subgraph structures with in a graph structure constructed for a plurality of executable instructions)", and p. 148 col. R:8-10, "an alternative approach would be

to compress repeated fragments (i.e. identify and optimize instructions) prior to register allocation"),

- identifying a plurality of unifiable variables within each fork subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions (p. 140 col. L:8-9, "our compression framework first identifies repeats (i.e. unifiable variables/instructions)", and p. 140 col. R:38-39, "the compiler must analyze them to identify any conditions that would inhibit the transformation (i.e. the unifiable variables/instructions that are not used simultaneously are identified for optimization)"),

- identifying at least one unifiable instruction of said plurality of executable instructions, within said plurality of fork subgraph structures (p. 140 col. R:38-39, "the compiler must analyze them to identify any conditions that would inhibit the transformation (i.e. the unifiable variables/instructions that are not used simultaneously are identified for optimization)"),

- transferring at least one unifiable instruction of said plurality of executable instructions from a fork of a corresponding fork subgraph structure of said plurality of fork subgraph structures to a handle of said corresponding fork subgraph structure (p. 141 col. R:27-29, "identical regions (unifiable instructions from a fork) that end with a jump to the same target are merged together (in the handle)"),

- said at least one unifiable instruction containing at least one unifiable variable of said plurality of unifiable variables (p. 140 col. L:8-9, "our compression framework first identifies repeats (i.e. unifiable variables/instructions)").

Cooper doesn't explicitly disclose **constructing a dependence graph of said plurality of executable instructions and using said dependence graph to** optimize code execution.

However, Damron in an analogous environment, discloses **constructing a dependence graph of said plurality of executable instructions and using said dependence graph to** optimize code execution (col. 4:60-65, "As is well known in the art dependency graph, and in particular directed acyclic graphs (DAGs), are commonly used to map or graph dependencies between instructions. Dependency graph have been used in the past to help optimize instruction scheduling for processor pipelines, or processors with multiple execution units").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Damron into the system of Cooper to have **constructing a dependence graph of said plurality of executable instructions and using said dependence graph to** optimize code execution. The modification would have been obvious because one of ordinary skill in the art would have wanted to use the well known and well document dependence graph to efficiently locate sections of code that are ideal for optimization.

As per claim 2, the rejection of claim 1 is incorporated and further, Cooper discloses that identifying said plurality of unifiable variables further comprises:

- constructing an interference graph structure for a plurality of local variables within said each fork subgraph structure (p. 143 col. R:23-24, "we first (construct and) use the interference graph),

- said plurality of local variables including said plurality of unifiable variables (p. 140 col. L:8-9, "our compression framework first identifies repeats (i.e. unifiable variables/instructions)"),

- identifying said plurality of unifiable variables as variables having non-overlapping live ranges within said interference graph structure (p. 143 figure 8, Live range analysis, and associated text (e.g. p. 143 col. L:34 – p. 144 col. R:42).

As per claim 3, the rejection of claim 2 is incorporated and further, Cooper discloses that **said interference graph structure indicates which variables of said plurality of local variables are simultaneously used in said plurality of executable instructions and cannot be unified** (p. 143 figure 8, Live range analysis, and associated text (e.g. p. 143 col. L:34 – p. 144 col. R:42), and p. 140 col. R:38-39, "the compiler must analyze them to identify any conditions that would inhibit the transformation (i.e. the unifiable variables/instructions that are not used simultaneously are identified for optimization)").

As per claim 4, the rejection of claim 1 is incorporated and further, Cooper discloses that identifying said plurality of unifiable variables further comprises: **constructing a data dependence** analysis **for said plurality of executable**

instructions; and identifying said plurality of unifiable variables using said data dependence analysis (p. 148 col. L:57-58, "(unifiable variables are identified) subject to (data) dependence constraints").

As per claim 5, the rejection of claim 1 is incorporated and further, Cooper discloses **initializing a flag for said at least one unifiable instruction; and unifying each unifiable variable within said at least one unifiable instruction** (p. 140 col. L:8-9, "our compression framework first identifies (i.e. flags) repeats (i.e. unifiable variables/instructions)", and p. 141 col. R:27-29, "identical regions (unifiable instructions from a fork) that end with a jump to the same target are merged together (in the handle)").

As per claim 6, the rejection of claim 5 is incorporated and further, Cooper discloses **removing said at least one unifiable instruction from subsequent forks of said corresponding fork subgraph structure** (p. 141 col. R:27-29, "identical regions (i.e. unifiable instructions) that end with a jump to the same target (are removed from a fork) are merged together (in the handle)").

As per claim 7, the rejection of claim 4 is incorporated and further, Cooper discloses that **said data dependence** analysis **contains a plurality of dependence arcs, each dependence arc connecting two instructions of said plurality of executable instructions contained within said fork of said corresponding fork**

subgraph structure (p. 148 col. L:57-58, "(unifiable variables are identified) subject to (data) dependence constraints").

As per claims 8-14, this is a system version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Cooper method of enhanced code compression for embedded RISC processors, p. 140 col. L:7-18 and Figs. 3 & 4, and the Damron system, col. 4:60-65.

As per claims 15-21, this is a computer readable medium version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Cooper method of enhanced code compression for embedded RISC processors, p. 140 col. L:7-18 and Figs. 3 & 4, and the Damron system, col. 4:60-65.

As per claims 22-28, this is another system version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Cooper method of enhanced code compression for embedded RISC processors, p. 140 col. L:7-18 and Figs. 3 & 4, and the Damron system, col. 4:60-65.

Response to Arguments

6. Applicants arguments have been considered but they are not persuasive.

In the remarks, the applicant has argued substantially that:

1) The cited art does not disclose identifying, prior to register allocation, a plurality of unifiable variables within each subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions, at p. 10:12-15, 11:14-20 and 13:8-9.

Examiner's response:

1) The examiner disagrees with applicant's characterization of the applied art. Cooper does disclose identifying, prior to register allocation, a plurality of unifiable variables within each subgraph structure of said plurality of fork subgraph structures, which are not simultaneously used in said plurality of executable instructions, at p. 143 col. R:23-24, "we first use the interference graph to (identify a plurality of fork subgraph structures with in a graph structure constructed for a plurality of executable instructions)", and p. 148 col. R:8-10, "an alternative approach would be to compress repeated fragments (i.e. identify and optimize instructions) prior to register allocation."

In the remarks, the applicant has argued substantially that:

2) One of ordinary skill in the art would not combine the teachings of Damron into the system of Cooper to construct a data dependence graph of said plurality of

executable instructions and using said graph to optimize code execution. The examiner has engaged in improper hind sight analysis, at p. 11:1-7, 11:27-12:19 and 13:10-18.

Examiner's response:

2) In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case, one of ordinary skill in the art would have wanted to use the well known and well document dependence graph to efficiently locate sections of code that are ideal for the desired type of optimization.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre R. Fowlkes whose telephone number is (571) 272-3697. The examiner can normally be reached on Monday - Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ARF

TUAN DAM
SUPERVISORY PATENT EXAMINER